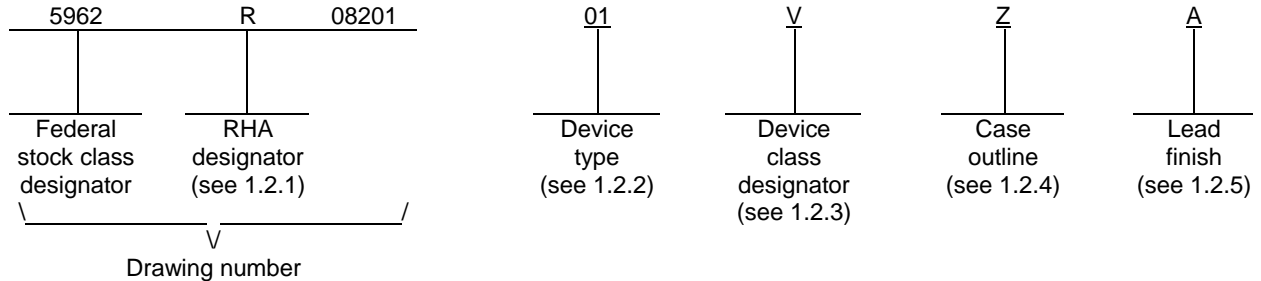


1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	AD768	16-bit, 30 MSPS, digital-to-analog converter

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
Z	CDFP3-F28	28	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Positive supply voltage (V_{DD}) with respect to DCOM, REFCOM, LADCOM pins	-0.5 V to +6.0 V
Negative supply voltage (V_{EE}) with respect to DCOM, REFCOM, LADCOM pins	-6.0 V to +0.5 V
Analog to other grounds (REFCOM) with respect to DCOM, LADCOM pins	-0.5 V to +0.5 V
Digital to other grounds (DCOM) with respect to LADCOM, REFCOM pins	-0.5 V to +0.5 V
Reference output (REFOUT) with respect to REFCOM pin	$V_{DD} + 0.5$ V maximum
Reference input current (IREFIN)	+7.5 mA maximum
Digital inputs (DB0 – DB15, CLOCK) with respect to DCOM pin	-0.5 V to $V_{DD} + 0.5$ V
Analog outputs (IOUTA, IOUTB) with respect to LADCOM pin	-2.0 V to +5.0 V
Maximum junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Lead temperature	+300°C
Thermal resistance, junction to ambient (θ_{JA})	50°C/W
Thermal resistance, junction to case (θ_{JC})	10°C/W

1.4 Recommended operating conditions.

Positive supply voltage (V_{DD})	+4.75 V dc to +5.25 V dc
Negative supply voltage (V_{EE})	-5.25 V dc to -4.75 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1.4.1 Operating performance characteristics.

Output resistance (R_{OUT})	1 k Ω
Output capacitance (C_{OUT})	12 pF
Output propagation delay (t_{PD})	17 ns
Output rise time (t_r)	5 ns
Output fall time (t_f)	5 ns
Output settling time to 0.025% (t_{ST})	35 ns
Input capacitance (C_{IN})	4 pF
Spurious free dynamic range within a window at 10 MSPS (SFDR _W)	86 dB
Spurious free dynamic range within a window at 30 MSPS (SFDR _W)	78 dB
Spurious free dynamic range to Nyquist at 10 MSPS (SFDR _N)	74 dB
Spurious free dynamic range to Nyquist at 30 MSPS (SFDR _N)	67 dB
Total harmonic distortion at 10 MSPS (THD)	-71 dB
Total harmonic distortion at 30 MSPS (THD)	-61 dB

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s)	100 krads(Si) 2/
--	------------------

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ This part may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Timing diagram. The timing diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/ 2/ 3/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution <u>4/ 5/</u>			4,5,6	01	16		Bits
Clock rate <u>4/ 5/</u>			4,5,6	01		30	MSPS
DC accuracy section							
Integral non-linearity <u>6/</u>	INL		4	01	-9	9	LSB
			5		-9	10	
			6		-13	12	
			M,D,P,L,R		4	-9	
Differential non-linearity <u>6/</u>	DNL		4	01	-11	7	LSB
			5		-9	8	
			6		-12	8	
			M,D,P,L,R		4	-11	
Analog output section							
Offset error <u>6/</u>	OE		1,2,3	01	-0.2	0.2	% of FSR
			M,D,P,L,R		1	-0.2	
Gain error <u>6/ 7/</u>	AE		1,2,3	01	-1.0	1.0	% of FSR
			M,D,P,L,R		1	-1.0	
Reference output section							
Reference voltage	V _{REF}		1,2,3	01	2.475	2.525	V
			M,D,P,L,R		1	2.475	
Reference output current <u>8/</u>	I _{OREF}		1,2,3	01		9.8	mA
			M,D,P,L,R		1		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/ 3/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Digital inputs section							
Logic "1" voltage	V _{IH}		1,2,3	01	3.5		V
			M,D,P,L,R		1	3.5	
Logic "0" voltage	V _{IL}		1,2,3	01		1.5	V
			M,D,P,L,R		1		
Logic "1" current	I _{IH}		1,2,3	01	-10	10	μA
			M,D,P,L,R		1	-10	
Logic "0" current	I _{IL}		1,2,3	01	-10	10	μA
			M,D,P,L,R		1	-10	
Input setup time	t _S		9,10,11	01	10		ns
			M,D,P,L,R		9	10	
Input hold time	t _H		9,10,11	01	5		ns
			M,D,P,L,R		9	5	
Latch pulse width	t _{LPW}		9,10,11	01	10		ns
			M,D,P,L,R		9	10	
Power supply section							
Positive supply current	I _{DD}		1,2,3	01		40	mA
			M,D,P,L,R		1		
Negative supply current	I _{EE}		1,3	01	-73		mA
			2		-75		
			M,D,P,L,R		1	-73	
Nominal power dissipation	P _D		1,2,3	01		600	mW
			M,D,P,L,R		1		
Power supply rejection ratio	PSRR	4.75 V < V _{DD} < 5.25 V, -5.25 V < V _{EE} < -4.75 V	4,6	01	-0.2	0.2	% of FSR / V
			5		-0.25	0.2	
			M,D,P,L,R		4	-0.2	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/ 2/ 3/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit	
					Min	Max		
AC linearity section. <u>9/</u>								
Spurious free dynamic range within a window	SFDR _W	F _{OUT} = 1.002 MHz, CLOCK = 20 MSPS	4,5,6	01	79		dB	
			M,D,P,L,R		4	79		
Spurious free dynamic range to Nyquist	SFDR _N	F _{OUT} = 1.002 MHz, CLOCK = 20 MSPS	4,6	01	65		dB	
					5	61		
			M,D,P,L,R		4	65		
Total harmonic distortion	THD	F _{OUT} = 1.002 MHz, CLOCK = 20 MSPS	4	01		-63	dB	
					5			-60
					6			-62
			M,D,P,L,R		4			-63

- 1/ Unless otherwise specified, V_{DD} = +5.0 V, V_{EE} = -5.0 V, LADCOM, REFCOM, and DCOM pins = 0 V, and IREFIN pin = 5 mA.
- 2/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, and R of irradiation. However, this device is tested only at the “R” level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.
- 3/ These parts may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Radiation end point limits for the noted parameters are guaranteed only for the conditions specified in MIL-STD-883, method 1019, condition A.
- 4/ Not tested post irradiation.
- 5/ Parameter tested as part of device initial characterization and after design and process changes.
- 6/ Measured at IOUTA and IOUTB, driving a virtual ground.
- 7/ Nominal full scale (FS) output current is 4 times the current at IREFIN. Therefore, nominal full scale current is 20 mA when IREFIN = 5 mA.
- 8/ Output current is defined as total current available IREFIN and any external load.
- 9/ Measured as unbuffered voltage output (1 V range) with full scale current into 50 Ω load on IOUTA and IOUTB.

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Device type	01
Case outline	Z
Terminal number	Test symbol
1	IOUTA
2	NR
3	REFOUT
4	NC
5	REFCOM
6	IREFIN
7	(LSB) DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	DCOM
16	CLOCK
17	DB8
18	DB9
19	DB10
20	DB11
21	DB12
22	DB13
23	DB14
24	DB15 (MSB)
25	V _{DD} (+5 v)
26	V _{EE} (-5 v)
27	IOUTB
28	LADCOM

FIGURE 1. Terminal connections.

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Terminal symbol	Type	Pin description
IOUTA	Analog output	Digital to analog converter (DAC) current output. Full scale current when all data bits are 1s.
NR	Analog input	Noise reduction node. Add capacitor for noise reduction.
REFOUT	Analog output	Reference output voltage. Nominal value is 2.5 V.
NC	NC	No connect. Reserved for internal use.
REFCOM	Power	Reference ground.
IREFIN	Analog input	Reference input current. Nominal is 5 mA. DAC full scale is 4 times this current
DB0	Digital input	Data bits 0, least significant bit (LSB).
DB1 – DB7	Digital input	Data bits 1 - 7.
DCOM	Power	Digital ground.
CLOCK	Digital input	Clock input. Data latched on positive edge of clock.
DB8 – DB14	Digital input	Data bits 8 – 14.
DB15	Digital input	Data bit 15, most significant bit (MSB).
V _{DD}	P	Positive supply voltage. Nominal is +5 V.
V _{EE}	P	Negative supply voltage, nominal is -5 V.
IOUTB	Analog output	Complementary DAC current output. Full scale current when all data bits are 0's.
LADCOM	Power	DAC ladder common.

FIGURE 1. Terminal connections – continued.

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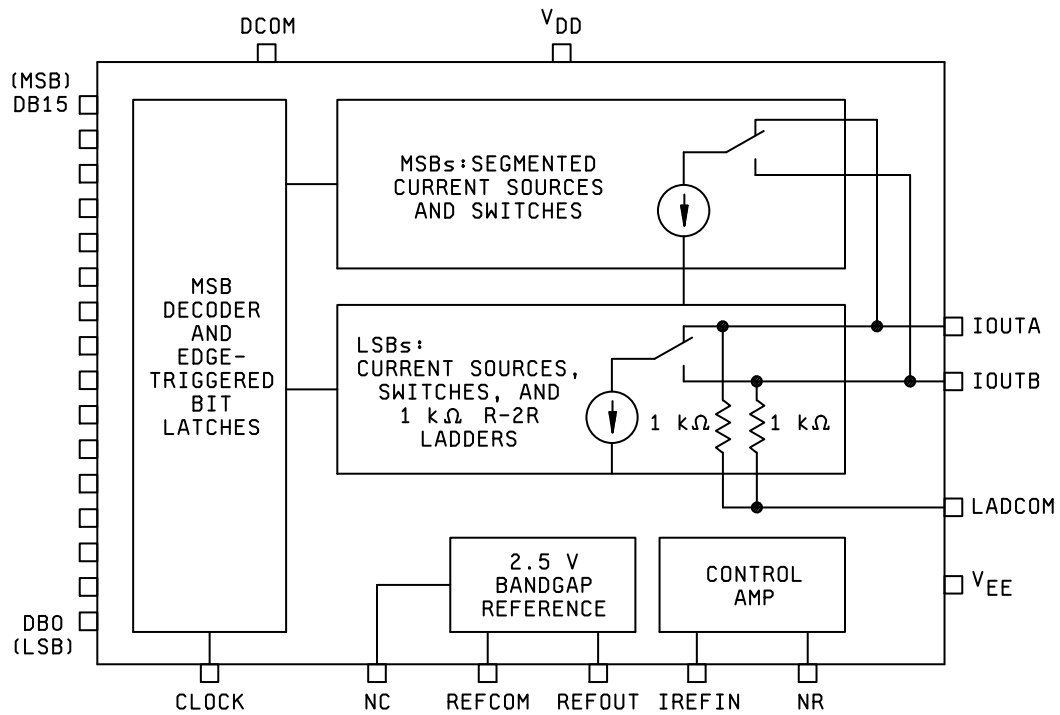


FIGURE 2. Block diagram.

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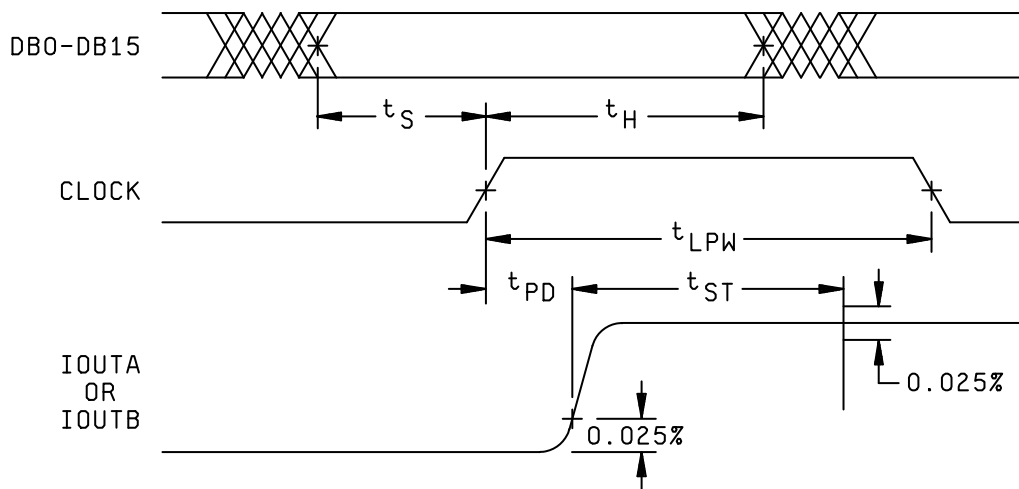


FIGURE 3. Timing waveforms.

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3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 92 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6, 1/ 9,10,11	1,2,3,4,5,6, 1/ 9,10,11	1,2,3,4, 1/ 2/ 5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6,9,10,11	1,2,3,4,5,6, 9,10,11	1,2,3,4,5,6, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1 2/
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9	1,4,9

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be computed with reference to the previous interim electrical parameters. Delta parameters are excluded from PDA.

TABLE IIB. 240 hour burn-in and group C end point electrical parameters.

Parameter	Delta limits	Units
I _{EE}	±3	mA
I _{DD}	±2	mA
V _{REF}	±0.0025	V
OE	±0.075	% of FSR
GE	±0.2	% of FSR

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

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4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-08201
		REVISION LEVEL	SHEET 15

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-01-30

Approved sources of supply for SMD 5962-08201 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R0820101VZA	24355	AD768AF/QMLR

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

24355

Vendor name and address

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: 7910 Triad Center
 Greensboro, NC 27409-9605

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.